Hittite Microwave

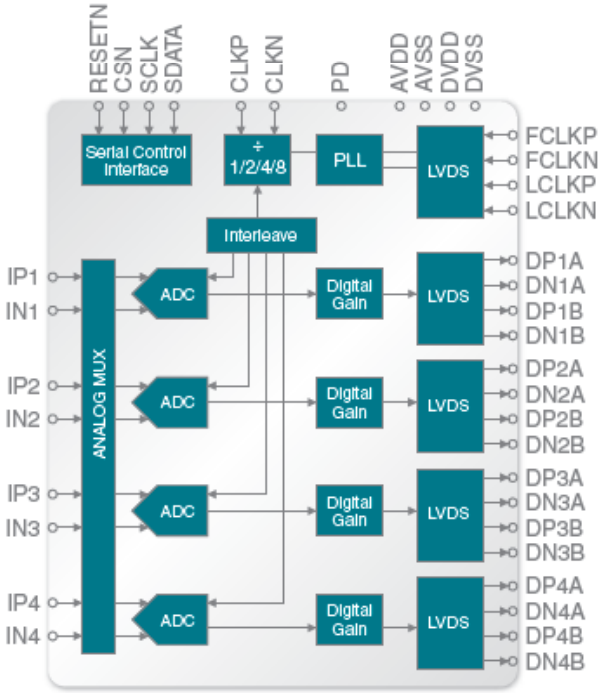
Single Chip RX and DPD solution featuring ADC: HMCAD1520 PLL: HMC830

HMCAD1520 – Multi-Mode ADC w/ Integrated Cross Point Switches

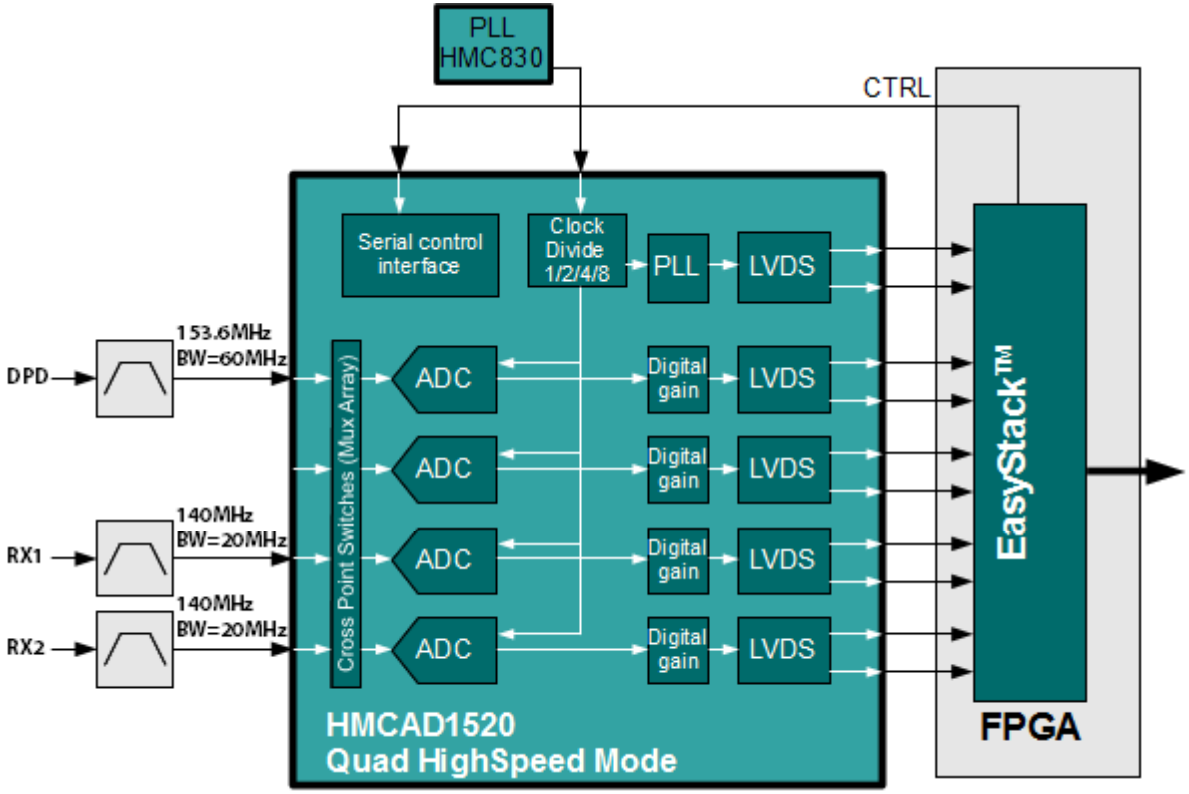
Part Number	Function / Mode	Resolution (bits)	Sample Rate (MSPS)	Power Dissipation[2][3]	SNR (dBFS)	SFDR (dBc)	Package
HMCAD1520	High Speed Single Channel	12	640	490 mW	70	60 / 75 [1]	LP7DE
	High Speed Dual Channel	12	320	490 mW	70	60 / 78 [1]	
	High Speed Quad Channel	12	160	490 mW	70	60 / 78 [1]	
	Precision Quad Channel	14	105	603 mW	74	83	
	Precision Quad Channel	14	80	530 mW	75	85	

Features

- ✓ *Multiple Modes*
  - ✓ *Single channel 12-bit up to 640 MSPS*
  - ✓ *Dual channel 12-bit up to 320 MSPS*
  - ✓ *Quad channel 12-bit up to 160 MSPS*
  - ✓ *Quad channel 14-bit up to 105 MSPS*
- ✓ *SPI Configurable Operational Modes*
- ✓ *SPI Configurable Number of Channels*
- ✓ *1µs Switching Time Between Configurations*
- ✓ *Internal 1X to 8X Clock Divider*
- ✓ *LVDS output*
  - ✓ *Full robustness inn RSDS (Low Current) Mode*
- ✓ *Ultra Low Power Dissipation*
  - ✓ *Dynamic power vs sample rate scaling*
- ✓ *Coarse & Fine Gain Control*
- ✓ *48 Pin QFN Package*



[1] Excluding Interleaving Spurs
[2] Supply Voltage (Vdd) +1.8 Vdc Analog Supply (Avdd) and +1.8Vdc Digital Supply (Dvdd)
[3] Output Supply Voltage (OVdd) +1.7 to +3.6 Vdc



HMCAD1520 and HMC830

- ✓ *High Speed Quad channel Mode: Sample rate up to 160MSPS available*
- ✓ *Recommended Sample rate: 125MSPS*
  - ✓ *14-bit LVDS mode available, giving 13-bit resolution at 125MSPS*
- ✓ *3 of 4 channels in use: Last channel can be put in Sleep mode to save power*
- ✓ *PLL: HMC830*
  - ✓ *Internal clock divider allows up to 1000MHz input ADC clock (125MSPS*8X)*
  - ✓ *Less than 200fsrms clock jitter in total clock path (including both PLL and ADC)*
- ✓ *FPGA Firmware: Hittite EasyStack™ FPGA firmware code available for Xilinx Spartan 6*

Measurement results
Board #1: Temp=25ºC

Setup: Quad Channel High speed mode

- ✓ *FS: **125 MSPS***
- ✓ *Fclk = **500MHz** (clock divide = 4)*
- ✓ *LVDS mode: **14-bit***
- ✓ *ADC Total Power Dissipation (inc. LVDS): **330 mW** - for 3 channels active (395 for 4 channels)*

- ✓ *SFDR caused by interleaving artifact. Two channels are sampling in antiphase with small time skew (~2ps) between them. Results in a spur at frequency $F_S/2-F_{IN.}$*
- ✓ *Interleaving spur not expected to affect the DPD algorithm*

Fin	Band	SNR*	SNDR	SFDR	HD2	HD3
140MHz	Nyquist	71.2dBFS	58.9dBFS	58.3dBc	91.7dBc	83.4dBc
140MHz	20MHz (130-150MHz)	75.8dBFS	75.6dBFS	93.2dBc	Out of Band	Out of Band
153.6MHz	Nyquist	71.4dBFS	59.7dBFS	59.1dBc	89.9dBc	88.3dBc

* SNR excluding Interleaving spurs

Measurement results
Board #2: Temp=-40ºC, 25ºC and 85ºC

Setup: Quad Channel High speed mode

- ✓ *FS: **125 MSPS***
- ✓ *Fclk = **500MHz** (clock divide = 4)*
- ✓ *LVDS mode: **14-bit***
- ✓ *ADC Total Power Dissipation (inc. LVDS): **330 mW** - for 3 channels active (395 for 4 channels)*

- ✓ *SFDR caused by interleaving artifact. Two channels are sampling in antiphase with small time skew (~2ps) between them. Results in a spur at frequency $F_S/2-F_{IN.}$*
- ✓ *Interleaving spur not expected to affect the DPD algorithm*

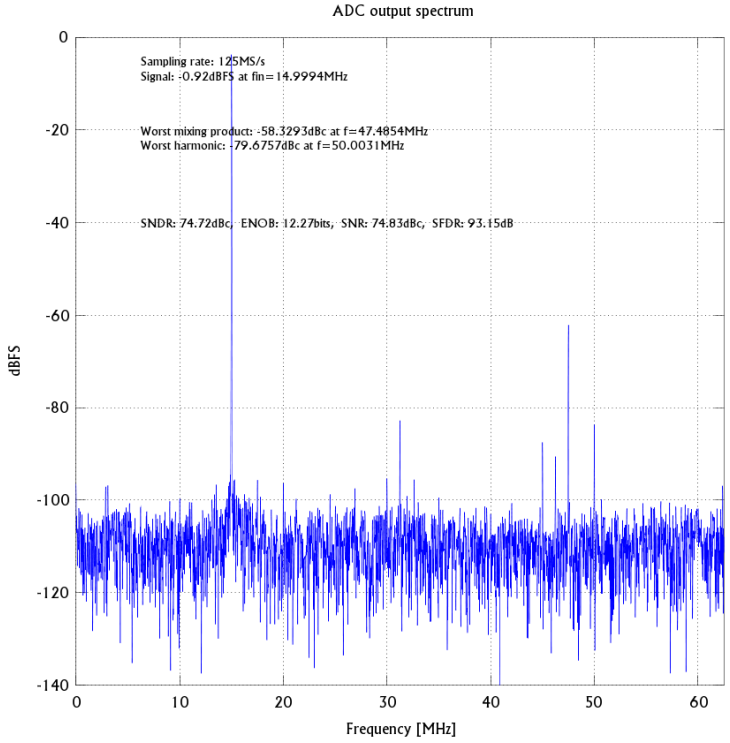
Fin	Band	Temp	SNR*	SNDR	SFDR	HD2	HD3
140MHz	Nyquist	-40ºC	69.9dBFS	62.5dBFS	62.8dBc	87.9dBc	81.3dBc
140MHz	Nyquist	25ºC	70.9dBFS	61.9dBFS	61.7dBc	87.4dBc	78.4dBc
140MHz	Nyquist	85ºC	70.5dBFS	60.3dBFS	59.7dBc	82.0dBc	76.3dBc
140MHz	**20MHz** (130-150MHz)	-40ºC	74.5dBFS	75.3dBFS	87.6dBc	Out of Band	Out of Band
140MHz	**20MHz** (130-150MHz)	25ºC	75.5dBFS	75.3dBFS	93.0dBc	Out of Band	Out of Band
140MHz	**20MHz** (130-150MHz)	85ºC	75.1dBFS	75.5dBFS	94.2dBc	Out of Band	Out of Band
153.6MHz	Nyquist	-40ºC	68.6dBFS	62.5dBFS	63.2dBc	93.5dBc	81.4dBc
153.6MHz	Nyquist	25ºC	69.6dBFS	62.3dBFS	62.4dBc	87.9dBc	82.4dBc
153.6MHz	Nyquist	85ºC	70.9dBFS	61.2dBFS	60.8dBc	83.7dBc	78.7dBc

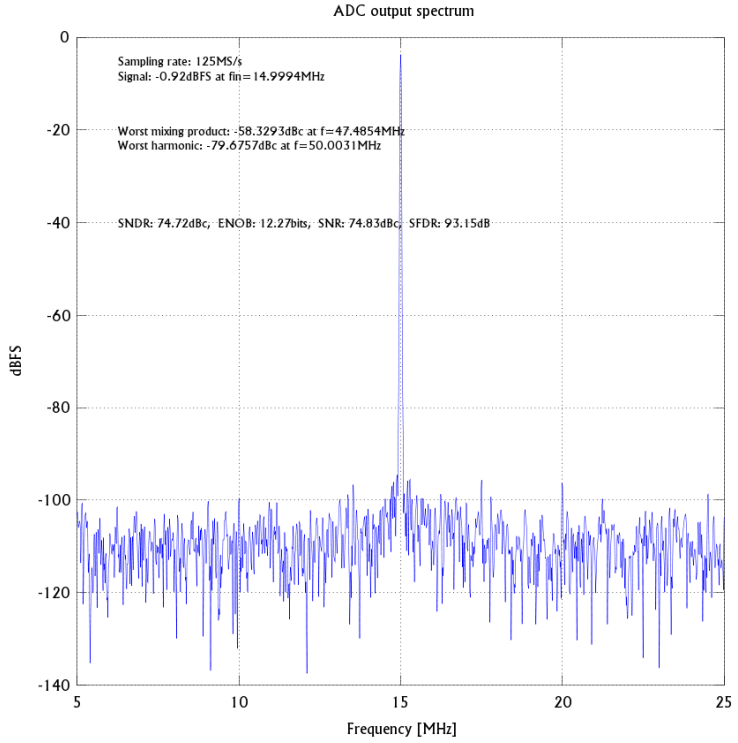
* SNR excluding Interleaving spurs

Ev.Board # FMC-301A-005

Setup: Quad Channel High speed mode

- ✓ ***FS**: 125MSPS*
- ✓ *Fclk = 500MHz (clock divide = 4)*
- ✓ *LVDS mode: 14-bit*





Full Nyquist band

- ✓ ***FS**: 125MSPS*
- ✓ *Fin: 140MHz folded to 15MHz*

20MHz (130-150MHz Band)

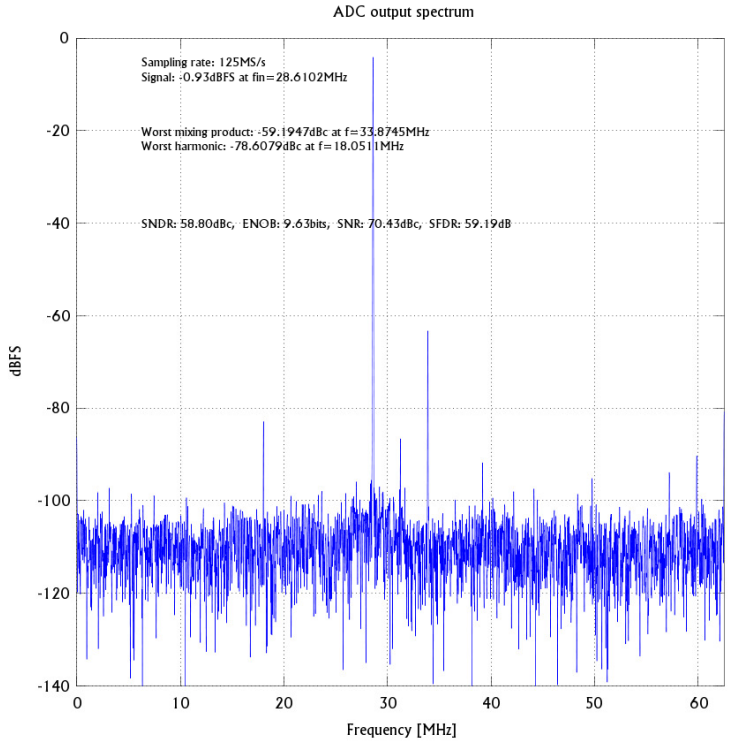
- ✓ ***FS**: 125MSPS*
- ✓ *Fin: 130-150 MHz folded to 5-25MHz*

FFT plot: Fin=153.6MHz, Temp=25ºC

Setup: Quad Channel High speed mode

- ✓ ***FS**: 125MSPS*
- ✓ *Fclk = 500MHz (clock divide = 4)*
- ✓ *LVDS mode: 14-bit*

- ✓ *HD2: -89.9 dBc*
- ✓ *HD3: -88.3 dBc*
- ✓ *HD5: -78.6 dBc*
- ✓ *HD7: -92.9 dBc*
- ✓ *HD9: -95.1 dBc*



Full Nyquist band

- ✓ ***FS**: 125MSPS*
- ✓ *Fin: 153.6MHz folded to 28.6MHz*

Recommended FPGA for HMCAD1520 based solution: Xilinx Spartan 6

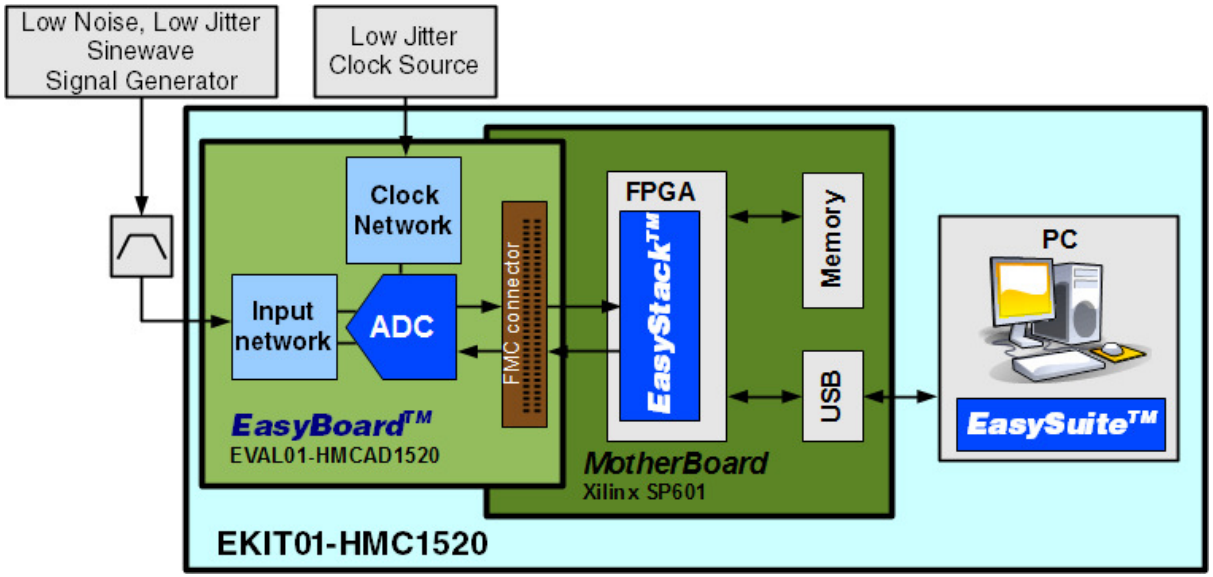
- ✓ *Low cost solution*
- ✓ *Size: Down to 8 mm x 8 mm*
- ✓ *Internal Memory: 24KSamples*

Hittite EasyStack: FPGA Firmware code stack

- ✓ *Available for Xilinx Spartan 6 as a part of HMCAD1520 offering*
- ✓ *EasyStack includes*
  - ✓ *HMCAD1520 LVDS receiver and De-serialization*
  - ✓ *HMCAD1520Configuration*
  - ✓ *USB data output*

Analog Made Easy™

- ✓ ***EasySuite™****: Evaluation and Prototyping Platform Environment*
  - ✓ *The EasySuite™ PC tool handles ADC configuration and ADC data analysis. With EasySuite™, the user can easily configure the ADC through the SPI port, perform measurements and analyse the result.*
  - ✓ *EasySuite™ includes Time-Interleave post processing, for Time-Interleave artifact analysis*
- ✓ ***EasyBoard™****: Supplied Evaluation Board Connected to Xilinx© Standard FMC Board*
- ✓ ***EasyStack™****: Firmware Code Stack, Currently Available for Xilinx©*
  - ✓ *EasyStack handles data transport over LVDS from the ADC to the FPGA, and from the FPGA to the PC.*
  - ✓ *EasyStack includes an ADC data processing API*



Hittite HMCAD1520&HMC830 measurements for RX and DPD:

- ✓ *RX and DPD ADC in one 7mm x 7mm package*
- ✓ *Very low Power Dissipation: Total 330 mW*
- ✓ *Below 200 fsrms total clock path jitter when used together with HMC830*
- ✓ *RX Performance: 140MHz Fin, 20MHz BW (130-150MHz)*
  - ✓ *75.6dB SNDR*
  - ✓ *93.2dB SFDR*
- ✓ *DPD Performance: 153.6Hz Fin*
  - ✓ *71.4dB SNR*
  - ✓ *89.9dB HD2*
  - ✓ *88.3dB HD3*
  - ✓ *59.1dB SFDR – Dominated by 2.5psrms interleaving spur which is not expected to affect the DPD algorithm*
- ✓ *Performance numbers stable over full -40 to +85ºC temperature range*
- ✓ *Firmware (EasyStack) to utilize low-cost high performance FPGA: Xilinx Spartan6*
- ✓ *Evaluation kit to configure, measure and analyze ADC*